What is claimed is:

1. An apparatus comprising:

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to an output terminal in synchronization with a first phase of a clock signal and communicate indications of the second data to the output terminal in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the output terminal in synchronization with the first phase and prevent communication of the second data during the second phase.

2. The apparatus of claim 1, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

3. The apparatus of claim 2, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

4. The apparatus of claim 2, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

5. The apparatus of claim 4, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

6. The apparatus of claim 5, wherein the logic does not provide the clock signal to the second latch in the second mode.

7. The apparatus of claim 5, wherein the logic comprises:

an AND gate including a first input terminal to receive a mode select signal, a second input terminal to receive the clock signal and an output terminal coupled to a clock input terminal of the second latch.

8. The apparatus of claim 2, further comprising:

a multiplexer including an output terminal that is coupled to the output terminal of the apparatus, the multiplexer alternatively selecting the first and second latch in response to the first and second phases of the clock signal.

9. The apparatus of claim 1, wherein the apparatus comprises a double pumped bus circuit.

10. A computer system comprising:

a system memory; and

a processor coupled to system memory, the processor including:

a wire;

a first circuit to receive indications of first data associated with a first data set and second data associated with a second data set; and

a second circuit coupled to the first circuit to cause the first circuit to:

in a first mode, communicate indications of the first data to the wire synchronization with a first phase of a clock signal and communicate indications of the second data to the wire in synchronization with a second phase of the clock signal, and

in a second mode, communicate the indications of the first data to the wire in synchronization with the first phase and prevent communication of the second data during the second phase.

11. The computer system of claim 10, wherein the first circuit comprises:

a first latch to store at least one bit at a time of the first data; and

a second latch to, at least in the first mode, store at least one bit at a time of the second data.

12. The computer system of claim 11, wherein the first latch transfers said at least one bit of the first data in response to a predefined edge of the clock signal.

13. The computer system of claim 11, wherein, in the first mode, the second latch transfers said at least one bit of the second data in response to a predefined edge of the clock signal.

14. The computer system of claim 13, further comprising:

logic to selectively provide the clock signal to the second latch based on whether the apparatus is in the first or second mode.

15. A system comprising:

double pumped bus circuits serially coupled together to form a chain to communicate data from at least two different sets of data, at least one of the bus circuits being capable of being disabled to prevent bits from at least one of the sets of data from being communicated through said at least one of the bus circuits.

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~~16. The system of claim 15, wherein alternate double pumped circuits are disabled to prevent the bits from at least one of the sets of data form being communicated through said at least one of the bus circuits.~~

17. The system of claim 15, wherein each double pumped circuit latches bits from one of the sets of data in response to first edges of a clock signal and furnishes indications of the bits in response to second edges of the clock signal, the first edges being different from the second edges.

18. The system of claim 17, wherein the first edges comprises positive edges of the clock signal.

19. The system of claim 17, wherein the first edges comprises negative edges of the clock signal.

20. A method comprising:

receiving first indications of first data associated with a first data set;

receiving second indications of second data associated with a second data set;

in a first mode, communicating the first indications to a double pumped bus in synchronization with a first phase of a clock signal and communicating the second indications to the double pumped bus in synchronization with a second phase of the clock signal; and

in a second mode, communicating the first indications to the double pumped bus in synchronization with the first phase and preventing communication of the second indications to the double pumped bus during the second phase.

21. The method of claim 20, wherein the receiving the first indications comprises:

latching the first indications one bit at a time.

22. ~~The method of claim 20, wherein the receiving the second indications comprises:~~

~~latching the second indications one bit at a time.~~

23. The method of claim 20, wherein the communicating during the first mode comprises:

communicating bits of the first data in response to first predefined edges of the clock signal; and

communicating a bits of the second data in response to other predefined edges of the clock signal, said other predefined edges being different from the first predefined clock edges.